AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

Listing of Claims:

Claim 1 (Original): A capacitance measurement circuit comprising:

first, second and third terminals, said first terminal being accompanied by a first capacitance including first and second capacitance components to be measured and a non-target capacitance component not to be measured, said third terminal being accompanied by a dummy capacitance having the same capacitance value as said non-target capacitance component;

a first current detector detecting a first current supplied to said first terminal;

a second current detector detecting a second current induced from said second terminal;

a third current detector detecting a third current supplied to said third terminal; and

a target capacitance forming section formed between said first terminal and said second terminal so that said first terminal is accompanied by said first capacitance component,

said target capacitance forming section, said first to third terminals, and said first to third current detectors constituting a capacitance measurement section.

Claim 2 (Original): The capacitance measurement circuit according to claim 1, wherein

said first to third current detectors include at least one transistor,

said at least one transistor including a transistor which has a transistor characteristic of being less apt to cause a leakage current than an ordinary transistor which constitutes a logic circuit.

Claim 3 (Original): The capacitance measurement circuit according to claim 1, wherein

said first to third current detectors include at least one transistor of a first conductivity type,

said at least one transistor being formed in a well region of a second conductivity type,

said well region being selectively formed in an upper layer of a bottom region of the first conductivity type.

Claim 4 (Original): The capacitance measurement circuit according to claim 1, wherein

said first to third current detectors include first and second transistors of different conductivity types,

said first and second transistors being formed in a semiconductor layer of an SOI substrate which is formed of a buried insulating layer and said semiconductor layer formed on said buried insulating layer,

said first and second transistors being isolated from each other by an element isolation region which extends to said buried insulating layer.

Claim 5 (Original): The capacitance measurement circuit according to claim 1, wherein

said capacitance measurement section includes first and second circuits,

said first and second circuits each comprising said first to third terminals and said first to third current detectors,

said first and second circuits respectively including, as said target capacitance forming section, first and second target capacitance forming sections which are different from each other,

said first capacitance component includes first and second partial capacitance components,

said first target capacitance forming section substantially includes said first and second partial capacitance components, and

said second target capacitance forming section substantially includes only said second partial capacitance component.

Claim 6 (Original): The capacitance measurement circuit according to claim 5, wherein

said first and second target capacitance forming sections include first and second measurement transistors, respectively,

said first and second measurement transistors each having a gate electrode and a pair of electrode regions, said gate electrode being electrically connected to said second terminal, one of said pair of electrode regions being electrically connected to an interconnect layer which is electrically connected to said first terminal,

said first partial capacitance component includes a coupling capacitance formed between said contact hole and said gate electrode,

said second partial capacitance component includes a coupling capacitance formed between said gate electrode and said interconnect layer,

in said first measurement transistor, a distance from said gate electrode to said contact hole is set to a length with which said first partial capacitance component is effective, and

in said second measurement transistor, a distance from said gate electrode to said contact hole is set to a length with which said first partial capacitance component is ineffective.

Claim 7 (Original): The capacitance measurement circuit according to claim 5, wherein

said first and second target capacitance forming sections include first and second measurement transistors, respectively,

said first and second measurement transistors each having a gate electrode, and first and second electrode regions which are electrically connected through first and second contact holes to first and second interconnect layers which are electrically connected to said first and second terminals, respectively,

said first partial capacitance component includes a coupling capacitance formed between said first and second contact holes,

said second partial capacitance component includes a coupling capacitance formed between said first and second electrode regions,

in said first measurement transistor, said first and second contact holes are formed such that said first partial capacitance component is effective, and

in said second measurement transistor, at least one of said first and second contact holes is formed such that said first partial capacitance component is zero.

Claim 8-29 (Cancelled).